

CLAIMS

What is claimed is:

- 1 1. A method comprising:  
2 predicting a next micro-operation address;  
3 storing the predicted address into a first memory;  
4 retrieving the predicted address from the first memory;  
5 accessing a second memory at the retrieved address to get a next micro-  
6 operation.  
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- 1 2. The method of claim 1, wherein storing the predicted address comprises  
2 programming the address into a read-only memory.  
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- 1 3. The method of claim 1, further comprising determining whether the micro-  
2 operation address is correctly predicted.  
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- 1 4. The method of claim 3, further comprising correcting the predicted address if  
2 the address is mispredicted.  
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- 1 5. The method of claim 4, wherein the next micro-operation indicates whether  
2 there is a jump present.  
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- 1 6. The method of claim 5, wherein the next micro-operation comprises one or  
2 more jump bits.  
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1 7. The method of claim 6, wherein determining whether the address is correctly  
2 predicted comprises checking the jump bit of the next micro-operation.

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1 8. The method of claim 7, wherein the next micro-operation address comprises a  
2 plurality of bits.

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1 9. The method of claim 8, wherein determining whether the address is correctly  
2 predicted further comprises checking the two least significant bits of the next micro-  
3 operation address to determine if a jump was executed.

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1 10. The method of claim 9, wherein correcting the predicted address comprises  
2 zeroing out the two least significant bits of the next micro-operation address.

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1 11. The method of claim 1, further comprising storing the next micro-operation for  
2 use in an instruction pipeline.

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1 12. The method of claim 11, wherein storing the next micro-operation comprises  
2 writing the micro-operation into a register.

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1 13. A system comprising:  
2 a first memory to store microcode, wherein the first memory is accessed at a  
3 next address to get a next micro-operation;  
4 a second memory to store predicted micro-operation addresses;  
5 misprediction recovery logic coupled to the first memory to determine if the  
6 predicted address is correct and to determine a recovery address; and  
7 a selector coupled to the first memory, the second memory, and the  
8 misprediction recovery, to select either the predicted address or the recovery address

9 as the next address at which to access the first memory based on the determination  
10 by the misprediction recovery logic as to whether the predicted address is correct.

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1 14. The system of claim 13, wherein the misprediction recovery logic to determine  
2 if the predicted address is correct comprises the misprediction recovery logic to  
3 determine whether there is a jump present and whether a jump was executed.

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1 15. The system of claim 14, wherein each address comprises a plurality of bits.

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1 16. The system of claim 15, wherein the next micro-operation comprises at least  
2 one jump bit.

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1 17. The system of claim 16, wherein the misprediction recovery logic to determine  
2 whether there was a jump present comprises the misprediction recovery logic to  
3 check the jump bit of each micro-operation.

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1 18. The system of claim 17, wherein the misprediction recovery logic to determine  
2 whether there was a jump executed comprises the misprediction recovery logic to  
3 check the two least significant bits of the next address.

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1 19. The system of claim 18, wherein the misprediction recovery logic to determine  
2 the recovery address comprises the misprediction recovery logic to zero out the two  
3 least significant bits of the next address.

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1 20. The system of claim 19, wherein the misprediction recovery logic to determine  
2 the recovery address further comprises the misprediction recovery logic to add the  
3 number of micro-operations per line to the next address.

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1 21. The system of claim 13, further comprising a register coupled to the first  
2 memory to store the next micro-operation.

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1 22. The system of claim 13, further comprising a register coupled to the first  
2 memory to store the next address for use by the misprediction recovery logic.

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1 23. The system of claim 13, wherein the selector is a multiplexer.

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1 24. A method comprising:  
2 predicting a next micro-operation address;  
3 determining a recovery address;  
4 determining whether the predicted address is correct;  
5 selecting between the predicted address and the recovery address based on  
6 whether the predicted address is correct; and  
7 accessing a memory with the selected address to get the next micro-operation.

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1 25. The method of claim 24, further comprising storing the predicted address.

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1 26. The method of claim 25, wherein storing the predicted address comprises  
2 storing the predicted address in a read-only memory.

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1 27. The method of claim 24, wherein determining whether the predicted address is  
2 correct comprises determining whether there is a jump present and whether a jump  
3 was executed.

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1 28. The method of claim 24, wherein the memory stores microcode.

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1 29. The method of claim 24, further comprising storing the next micro-operation.

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1 30. The method of claim 24, further comprising storing the selected address.